DEVICE HAVING SLOPED GATE PROFILE AND METHOD OF MANUFACTURE

BACKGROUND

Semiconductor devices are used in a variety of electronic applications, such as personal computers, cell phones, digital cameras, and other electronic equipment, as examples. Semiconductor devices are typically fabricated by sequentially depositing insulating or dielectric layers, conductive layers, and semiconductive layers of material over a semiconductor substrate, and patterning the various material layers using lithography to form circuit components and elements thereon.

Transistors are circuit components or elements that are often formed on semiconductor devices. Many transistors may be formed on a semiconductor device in addition to capacitors, inductors, resistors, diodes, conductive lines, or other elements, depending on the circuit design. A field effect transistor (FET) is one type of transistor.

Generally, a transistor includes a gate stack formed between source and drain regions. The source and drain regions may include a doped region of a substrate and may exhibit a doping profile suitable for a particular application. The gate stack is positioned over the channel region and may include a gate dielectric interposed between a gate electrode and the channel region in the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIGS. **1-5** illustrate various intermediate stages of forming a semiconductor device in accordance with some embodiments.

FIG. **6** is a flow diagram illustrating a method of forming a semiconductor device, in accordance with some embodiments.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

Embodiments are discussed below with reference to forming a gate electrode using a gate-last approach for illustrative purposes. Generally, a dummy gate electrode having gate spacers formed along sidewalls of the dummy gate electrode is formed. The dummy gate electrode is removed and a process is performed to widen an upper portion of the opening formed by the removal of the dummy gate electrode, thereby forming a funnel-shaped opening. The gate electrode is formed in the funnel-shaped opening, thereby providing a gate electrode having an open profile. The funnel-shaped opening reduces or prevents voids that may occur during the formation of the gate electrode. Other embodiments may utilize other processes to form the open profile gate electrode.

FIGS. **1-5** illustrate various intermediate stages of an embodiment of forming a gate electrode in accordance with some embodiments. Referring first to FIG. **1**, there is shown a substrate **102** having a dummy gate stack **104** formed thereon. The substrate **102** may comprise, for example, bulk silicon, doped or undoped, or an active layer of a semiconductor-on-insulator (SOI) substrate. Generally, an SOI substrate comprises a layer of a semiconductor material, such as silicon, silicon germanium, silicon carbide, or the like, formed on an insulator layer. The insulator layer may be, for example, a buried oxide (BOX) layer or a silicon oxide layer. The insulator layer is provided on a substrate, typically a silicon substrate or glass substrate. Other substrates, such as multi-layered or gradient substrates may also be used.

As discussed in greater detail below, the dummy gate stack **104** is a sacrificial structure used to align and form source/drain regions **106** adjacent to the dummy gate stack **104** and will be replaced in subsequent processing steps. As such, the dummy gate stack **104** may be formed of any suitable material and processes. In some embodiments, the dummy gate stack **104** is formed simultaneously as other devices on the wafer, such as other transistors. In these embodiments, it may be desirable to form the dummy gate stack **104** from a dummy gate dielectric **104***a* and a dummy gate electrode **104***b*, which layers may be used to form functional gate stacks for other devices.

The source/drain regions **106** may include any appropriate doping profile for a particular application. For example, the source/drain regions **106** may include lightly-doped source/drain (LDD) regions formed by implanting dopants, e.g., n-type dopants or p-type dopants, using the dummy gate stack **104** as a mask, thereby aligning the LDD regions with the edges of dummy gate stack **104**. Halo and/or pocket regions (not shown) may also be formed.

FIG. **1** further illustrates the formation of one or more spacers **108** in accordance with an embodiment. FIG. **1** illustrates an embodiment in which the spacers **108** include first gate spacers **108***a* and second gate spacers **108***b* (collectively referred to as "spacers **108**") along sidewalls of the dummy gate stack **104**. The second gate spacers **108***b* may also act as a contact etch stop layer (CESL) during formation of contacts through a subsequently formed interlayer dielectric film.

As explained in greater detail below, the spacers **108** will be etched to form a funnel-shaped opening during the removal of the dummy gate stack **104**, thereby allowing an